*Click **here** to ask an associate for production status of specific part numbers.*

# MAX16163/MAX16164

# nanoPower On/Off Controller with Programmable Sleep Time

## General Description

The MAX16163 and MAX16164 are nanopower on/off controllers with programmable sleep time. The devices integrate a power switch to gate an output, which provides up to 200mA load current.

The MAX16163/MAX16164 use either an external resistor to program the sleep time or program the sleep time through an $I^2C$ bus. When the device powers up, it checks the connection on the PB/SLP pin; if the resistance between the PB/SLP pin and ground is larger than 5.5MΩ, the device is configured as $I^2C$ programmable. Otherwise, the device is configured as resistor programmable.

When the MAX16163 powers up, it measures the resistance on the PB/SLP pin to the ground and sets the sleep time properly. It then asserts the OUT output. When the downstream device (e.g., a µC) finishes its task, it asserts a falling edge on the CLRB pin; the MAX16163 then deasserts OUT and the sleep timer starts. When the sleep timer expires, the MAX16163 asserts OUT again.

When the MAX16164 powers up, it measures the resistance on the PB/SLP pin to the ground and sets the sleep time properly. It then keeps OUT deasserted and puts the device in SHUTDOWN state. The MAX16164 does not assert OUT until a pushbutton closure on the PB/SLP pin.

The MAX16163/MAX16164 operate over the -40°C to +125°C temperature range and are available in a 1.54mm x 1.11mm, 6-bump thin wafer-level package (WLP) and a 6-pin µDFN package.

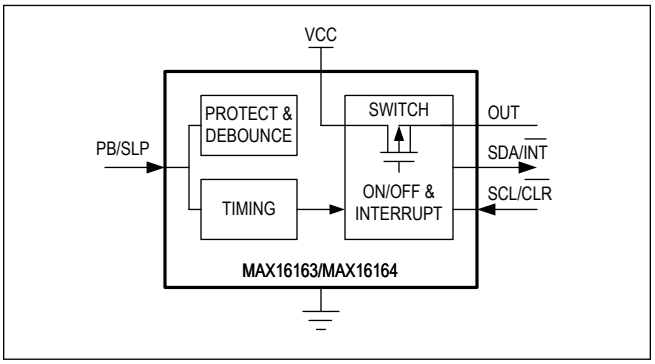
## Applications

- Battery-Powered Equipment
- Remote Sensors
- Internet of Things (IoT)
- Portable Instruments
- Handheld Consumer Electronics
- Industrial Equipment
- Disposable Low-Power Electronics

## Benefits and Features

- Ultra Low Current Saves Power
  - 30nA $I_Q$ in SLEEP_TIMER State
  - 10nA $I_Q$ in SHUTDOWN State
  - VCC Range: 1.7V to 5.5V
- Robust Features Increases End Equipment Reliability
  - Pushbutton Input Handles up to ±60V
  - ±40kV HBM ESD Protection
- Flexible Configurations Provide Design Options
  - $I^2C$ or Resistor Programmable Sleep Time
  - Interrupt Output and Clear Input in Resistor Programmable Configuration
  - Up to 32 Different Sleep Time Values from 100ms to 24 Hours, and Infinite
  - Latched Output Supplies 200mA Load Current With Less Than 30mV Drop

## Simplified Block Diagram




*Ordering Information appears at end of data sheet.*

19-101175; Rev 1; 10/21

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## Absolute Maximum Ratings

$V_{CC}$ to GND ..... -0.3V to +6V
PB/SLP to GND ..... -60V to +60V
SCL/CLR, SDA/INT, OUT to GND ..... -0.3V to +6V
Continuous Power Dissipation (Multilayer Board) 6-uDFN ($T_A$ = +70°C, derate 4.5mW/°C above +70°C) ..... 357.8mW
Continuous Power Dissipation (Multilayer Board) 6-WLP ($T_A$ = +70°C, derate 10.51mW/°C above +70°C) ..... 840.78mW
Junction Temperature ..... +150°C
Operating Temperature Range ..... -40°C to +125°C
Storage Temperature Range ..... -40°C to +150°C
Soldering Temperature (reflow) ..... +260°C

*Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

## Package Information

### 6 uDFN

| | |
|---|---|
| Package Code | L622+1C |
| Outline Number | 21-0164 |
| Land Pattern Number | 90-0004 |
| **Thermal Resistance, Four Layer Board:** | |
| Junction-to-Ambient ($\theta_{JA}$) | 223.6°C/W |
| Junction-to-Case Thermal Resistance ($\theta_{JC}$) | 122°C/W |

### 6 WLP

| | |
|---|---|
| Package Code | N61C1+1 |
| Outline Number | 21-100527 |
| Land Pattern Number | Refer to *Application Note 1891* |
| **Thermal Resistance, Four-Layer Board:** | |
| Junction-to-Ambient ($\theta_{JA}$) | 95.15°C/W |
| Junction-to-Case Thermal Resistance ($\theta_{JC}$) | N/A |

For the latest package outline information and land patterns (footprints), go to *www.maximintegrated.com/packages*. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to *www.maximintegrated.com/thermal-tutorial*.

## Electrical Characteristics

($V_{CC}$ = $V_{MIN}$ to $V_{MAX}$, $T_A$ = -40°C to +125°C, limits over the operating temperature range and relevant supply voltage range are guaranteed by production test and/or characterization. Typical values are at $T_A$ = +25°C and $V_{CC}$ = +3.3V)

| PARAMETER | SYMBOL | CONDITIONS | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|
| Operating Voltage Range | $V_{CC}$ | | | 1.7 | | 5.5 | V |
| Power Supply Current | $I_{SD}$ | $V_{CC}$ = 3.3V, OUT not asserted, PB/SLP not connected to pushbutton. SHUTDOWN state (MAX16164). | -40°C ≤ $T_A$ ≤ +70°C | | 10 | 40 | nA |
| | | | -40°C ≤ $T_A$ ≤ +85°C | | | 80 | |
| | $I_{SLP}$ | $V_{CC}$ = 3.3V, OUT not asserted, PB/SLP not connected to pushbutton. SLEEP_TIMER state. | -40°C ≤ $T_A$ ≤ +70°C | | 30 | 80 | |
| | | | -40°C ≤ $T_A$ ≤ +85°C | | | 200 | |
| | | | -40°C ≤ $T_A$ ≤ +105°C | | 150 | | |
| | $I_{CC}$ | During $R_{SLP}$ measurement | | | 265 | | µA |
| Input High Voltage | $V_{IH}$ | SCL/$\overline{CLR}$ , SDA, and PB/SLP | | 70 | | | %$V_{CC}$ |
| Input Low Voltage | $V_{IL}$ | SCL/$\overline{CLR}$ , SDA, and PB/SLP | | | | 30 | %$V_{CC}$ |
| Minimum Input High Time Detected | | PB/SLP | | | 50 | | ms |
| PB/SLP Hysteresis | | | | | 100 | | mV |
| PB/SLP Pulldown Resistance | | 0 < $V_{PB/SLP}$ < $V_{CC}$ | | 20 | | 100 | MΩ |
| PB/SLP Input Current | $I_{IN}$ | $V_{PB/SLP}$ = ±60V | | -6 | | +6 | mA |
| PB/SLP Voltage Range | | Continuous; 0V ≤ $V_{CC}$ ≤ 5.0V | | -60 | | +60 | V |
| | | Transient; 0V ≤ $V_{CC}$ ≤ 5.5V | | -60 | | +60 | |
| $\overline{CLR}$ Input Current | $I_{CLR}$ | | | -10 | ±1 | +10 | nA |
| $\overline{CLR}$ Falling Edge to OUT Falling Propagation Delay | $t_{CO}$ | $R_L$ = 10kΩ, $C_L$ = 100pF | | | 200 | | ns |
| $I^2C$ SHUTDOWN Command to OUT Falling Propagation Delay (Note 1) | | $R_L$ = 10kΩ, $C_L$ = 100pF | | 25 | | 65 | ms |
| $\overline{CLR}$ Lockout Time | | Period following rising edge of OUT during which transitions on $\overline{CLR}$ are ignored | | 70 | | | ms |
| OUT Output Voltage | $V_{OH}$ | $V_{CC}$ = 3.3V, $I_{SOURCE}$ = 200mA | | $V_{CC}$ - 0.03 | | | V |
| | | $V_{CC}$ = 2.0V, $I_{SOURCE}$ = 2mA | | $V_{CC}$ - 0.01 | | | |
| $\overline{INT}$ Output Voltage | $V_{OL\_INT}$ | $V_{CC}$ = 3.3V, $I_{SINK}$ = 1mA | | | | 0.2 | V |
| $\overline{INT}$ Leakage Current | | | | -10 | ±1 | +10 | nA |
| Pushbutton Debounce Time | $t_{DB}$ | | | 40 | | 90 | ms |

## Electrical Characteristics (continued)

($V_{CC}$ = $V_{MIN}$ to $V_{MAX}$, $T_A$ = -40°C to +125°C, limits over the operating temperature range and relevant supply voltage range are guaranteed by production test and/or characterization. Typical values are at $T_A$ = +25°C and $V_{CC}$ = +3.3V)

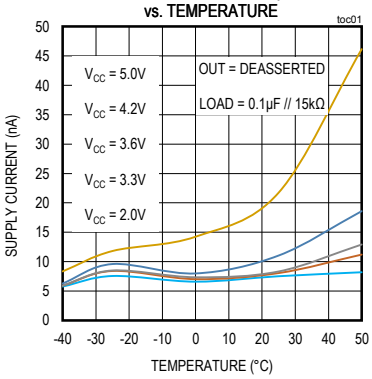
| PARAMETER | SYMBOL | CONDITIONS | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|
| Pushbutton Shutdown Period | $t_{SO}$ | | | 7.2 | 8 | 8.8 | s |
| Interrupt Pulse Duration | $t_{INT}$ | Beginning at the end of $t_{DB}$. | | 36 | 40 | 44 | ms |
| | | Beginning at the end of $t_{SO}$. | | | 4 x $t_{INT}$ | | |
| Sleep Time | $t_{SLP}$ | Beginning at $t_{SO}$ and button release or CLR falling edge. See Table 1. | | 100 | | | ms |
| | | Beginning at $t_{SO}$ and button release or CLR falling edge. See Table 1. | | | | 24 | hour |
| Sleep Time Accuracy | | | | | 5 | | % |
| Powerup Time Delay | | POR time plus resistance detection time | | | 120 | | ms |
| ESD Protection | | PB/SLP | Human Body Model | | ±40 | | kV |
| **I²C TIMING CHARACTERISTICS** | | | | | | | |
| Serial Clock Frequency (Note 1) | $f_{SCL}$ | Standard Mode | | 0 | | 100 | kHz |
| Bus Free Time Between STOP and START Conditions | $t_{BUF}$ | | | 4.7 | | | µs |
| Hold Time After Repeated START | $t_{HD:STA}$ | | | 4 | | | µs |
| SCL Clock Low Period | $t_{LOW\_I2C}$ | | | 4.7 | | | µs |
| SCL Clock High Period | $t_{HIGH\_I2C}$ | | | 4.0 | | | µs |
| Setup Time for a Repeated START Condition | $t_{SU:STA}$ | | | 4.7 | | | µs |
| Data Hold Time | $t_{HD:DAT}$ | | | -15 | | | ns |
| | | | | | | 3.45 | µs |
| Data Setup Time | $t_{SU:DAT}$ | | | 250 | | | ns |
| Setup Time for STOP Condition | $t_{SU:STO}$ | | | 4 | | | µs |
| Capacitive Load for Each Bus Line (Note 1) | $C_B$ | | | | | 400 | pF |
| SDA and SCL Rise Time | $t_{R\_I2C}$ | | | | | 1000 | ns |
| SDA and SCL Fall Time | $t_{F\_I2C}$ | | | | | 300 | ns |

**Note 1:** Guaranteed by design, not production tested.

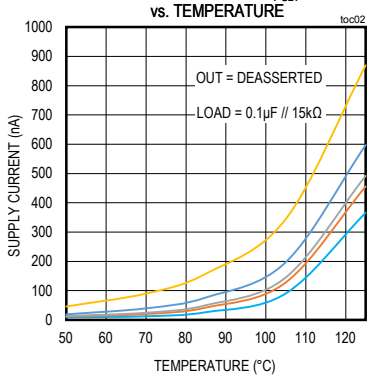
## Typical Operating Characteristics

($V_{CC}$ = +3.3V, $T_A$ = +25°C, unless otherwise noted.)

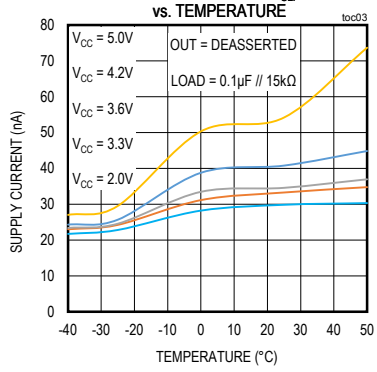
SUPPLY CURRENT ($I_{SD}$) vs. TEMPERATURE



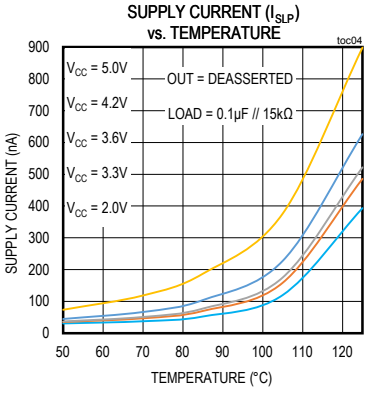

SUPPLY CURRENT ($I_{SD}$) vs. TEMPERATURE



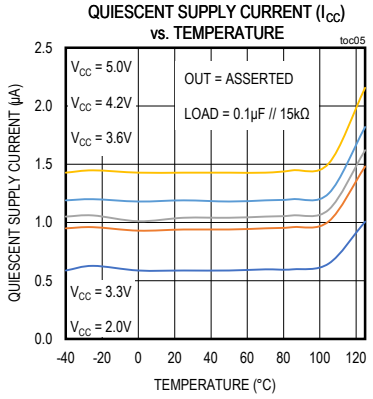

SUPPLY CURRENT ($I_{SLP}$) vs. TEMPERATURE



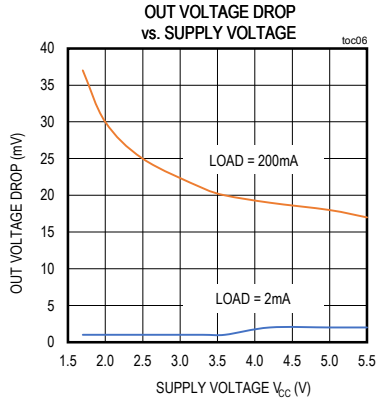

SUPPLY CURRENT ($I_{SLP}$) vs. TEMPERATURE



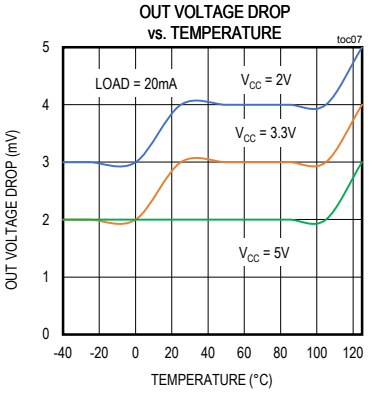

QUIESCENT SUPPLY CURRENT ($I_{CC}$) vs. TEMPERATURE



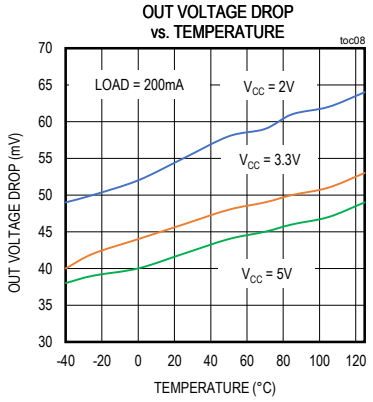

OUT VOLTAGE DROP vs. SUPPLY VOLTAGE



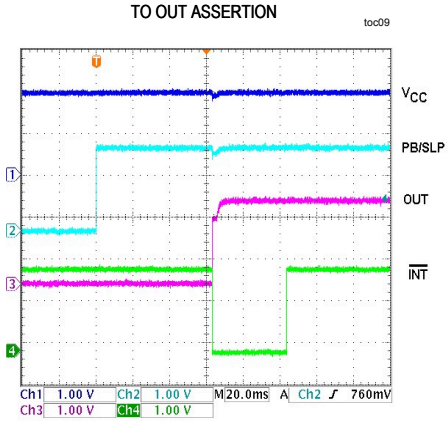

OUT VOLTAGE DROP vs. TEMPERATURE




OUT VOLTAGE DROP vs. TEMPERATURE

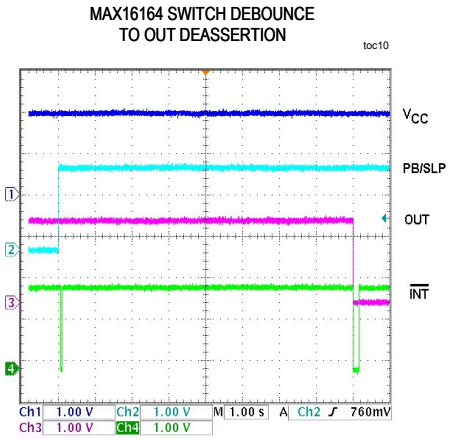



MAX16164 SWITCH DEBOUNCE TO OUT ASSERTION



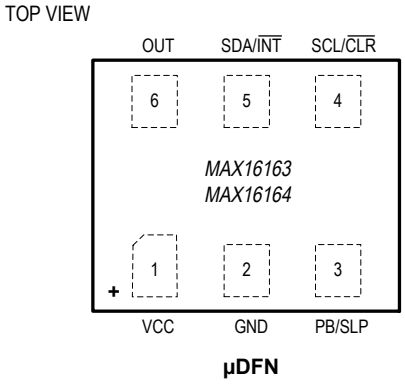
## Typical Operating Characteristics (continued)

($V_{CC}$ = +3.3V, $T_A$ = +25°C, unless otherwise noted.)

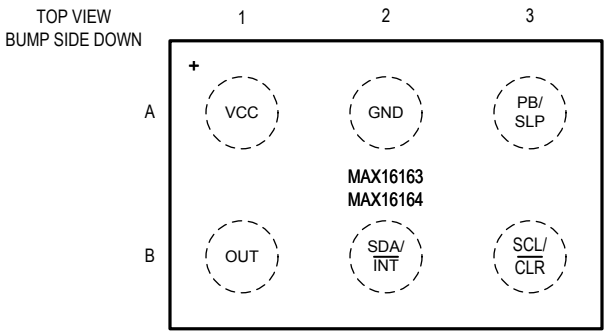



## Pin Configurations

### uDFN



### WLP




## Pin Description

| PIN | | NAME | FUNCTION |
|---|---|---|---|
| uDFN | WLP | | |
| 1 | A1 | $V_{CC}$ | Power Supply Input |
| 2 | A2 | GND | Ground |
| 3 | A3 | PB/SLP | Pushbutton Input and Sleep Time Configuration Resistor Connection. In the RES_CALC state, the resistance between this pin and GND is measured and used to set the sleep time $t_{SLP}$. PB/SLP is internally pulled down to GND through a 50MΩ resistor. Holding PB/SLP high for a period greater than the debounce time ($t_{DB}$) asserts OUT to high, and if the device is configured as resistor programmable, the device generates a one-shot pulse at $\overline{INT}$. Holding PB/SLP high for a period greater than the shutdown period ($t_{SO}$) deasserts OUT to low, and if the device is configured as resistor programmable, the device generates an extended pulse (4x $t_{INT}$) at $\overline{INT}$. |
| 4 | B3 | SCL/$\overline{CLR}$ | When the device is configured as $I^2C$ programmable, the pin is the $I^2C$ bus clock line.<br><br>When the device is configured as resistor programmable, the pin is clear input. Pulling $\overline{CLR}$ from high to low deasserts the latched OUT signal. If OUT is already deasserted when $\overline{CLR}$ is pulled low, the state of OUT is unchanged. |
| 5 | B2 | SDA/$\overline{INT}$ | When the device is configured as $I^2C$ programmable, the pin is the $I^2C$ bus data line.<br><br>When the device is configured as resistor programmable, the pin is active-low, open-drain interrupt/reset output. $\overline{INT}$ is a one-shot output pulse. $\overline{INT}$ asserts for the interrupt timeout period when PB/SLP is held high for a period greater than the debounce time ($t_{DB}$). $\overline{INT}$ asserts for four times the interrupt timeout period when PB/SLP is held high for a period greater than the shutdown period ($t_{SO}$). $\overline{INT}$ is high-impedance when deasserted, even when pulled above $V_{CC}$. |
| 6 | B1 | OUT | The source terminal of the internal MOSFET switch. OUT is connected to $V_{CC}$ through the MOSFET when asserted. OUT is disconnected from $V_{CC}$ when deasserted. |

## Detailed Description

The MAX16163 and MAX16164 are nanopower On/Off controllers with programmable sleep time. The devices integrate a power switch to gate an output, which provides up to 200mA load current.

The controllers have debounced pushbutton input to manually control the latched output. A button press that pulls PB/SLP high and is stable for a period greater than or equal to the debounce time ($t_{DB}$) causes OUT to assert high. A button press period greater than or equal to the shutdown period ($t_{SO}$) causes OUT to deassert low.

The MAX16163/MAX16164 use either an external resistor to program the sleep time or program the sleep time through an $I^2C$ bus. When the MAX16163/MAX16164 power up, they automatically check the resistance between the PB/SLP pin and ground; if the resistance is larger than 5.5MΩ, the device is configured as $I^2C$ programmable. Otherwise, the device is configured as resistor programmable.

Figure 1 shows the pin configurations for resistor programmable and $I^2C$ programmable sleep time. The resistor programmable pin configuration is shown in red, the $I^2C$ programmable pin configuration is shown in black.

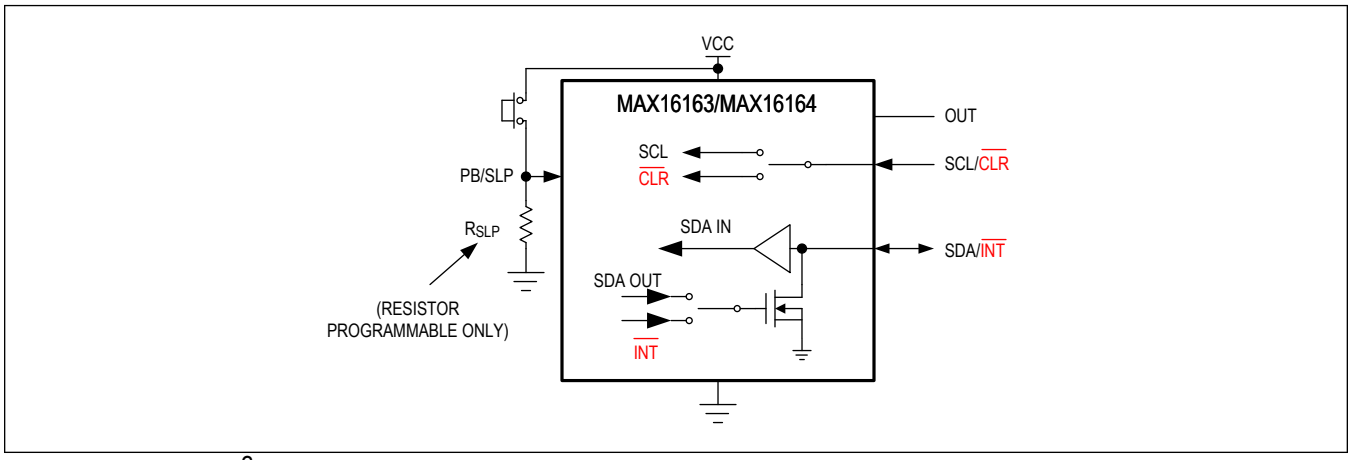



*Figure 1. Resistor and $I^2C$ Programmable Sleep Time Pin Configurations*

In the resistor programmable configuration and when OUT is asserted, a falling edge on the $\overline{CLR}$ pin at any time causes OUT to deassert. When OUT is deasserted, the $\overline{CLR}$ pin input is ignored. In this configuration, there is also an open-drain, active-low $\overline{INT}$ output, which is a mirrored output of the button press activity.

In the $I^2C$ programmable configuration, there are no $\overline{CLR}$ input pin and $\overline{INT}$ output pins, the pins are multiplexed as SCL and SDA pins respectively. The device deasserts OUT when an $I^2C$ SHUTDOWN command is received. The device also updates the sleep time when a new sleep time register value is received through the $I^2C$ bus.

The sleep time is programmed as shown in Table 1:

## Table 1. Sleep Time Programming in Resistor and I²C Configurations

| SLEEP TIME | SLEEP TIME REGISTER VALUE IN I²C PROGRAMMABLE CONFIGURATION | IDEAL $R_{SLP}$ VALUE (kΩ) IN RESISTOR PROGRAMMABLE CONFIGURATION | RECOMMENDED 1% TOLERANCE RESISTOR (kΩ) |
|---|---|---|---|
| 100ms | 0x00 | — | — |
| 200ms | 0x01 | — | — |
| 400ms | 0x02 | — | — |
| 600ms | 0x03 | — | — |
| 800ms | 0x04 | — | — |
| 1s | 0x05 | — | — |
| 2s | 0x06 | — | — |
| 4s | 0x07 | — | — |
| 6s | 0x08 | — | — |
| 8s | 0x09 | — | — |
| 10s | 0x0A | 960 | 953 |
| 20s | 0x0B | 807 | 806 |
| 40s | 0x0C | 678 | 681 |
| 1 min (default value in I²C programmable configuration) | 0x0D | 570 | 576 |
| 2 min | 0x0E | 480 | 475 |
| 4 min | 0x0F | 403 | 402 |
| 6 min | 0x10 | 339 | 340 |
| 8 min | 0x11 | 285 | 287 |
| 10 min | 0x12 | 240 | 243 |
| 20 min | 0x13 | 202 | 200 |
| 40 min | 0x14 | 169 | 169 |
| 1 hour | 0x15 | 143 | 143 |
| 2 hour | 0x16 | 120 | 121 |
| 4 hour | 0x17 | 101 | 100 |
| 6 hour | 0x18 | 84.9 | 84.5 |
| 8 hour | 0x19 | 71.4 | 71.5 |
| 10 hour | 0x1A | 60.0 | 60.4 |
| 12 hour | 0x1B | 50.5 | 49.9 |
| 16 hour | 0x1C | 42.4 | 42.2 |
| 20 hour | 0x1D | 35.7 | 35.7 |
| 24 hour | 0x1E | 30.0 | 30.1 |
| INFINITE | 0x1F | 25.2 | 25.5 |

## State Diagram

### MAX16163/MAX16164 State Diagram

The MAX16163/MAX16164 state diagram is shown in Figure 2. PB/SLP = 1 indicates that the PB/SLP pin is at high voltage, typically by pressing a pushbutton connected to $V_{CC}$. PB/SLP = 0 indicates that the pin is not pulled up to $V_{CC}$ by pressing a pushbutton. The PB/SLP pin has an internal 50MΩ resistor connected to ground.

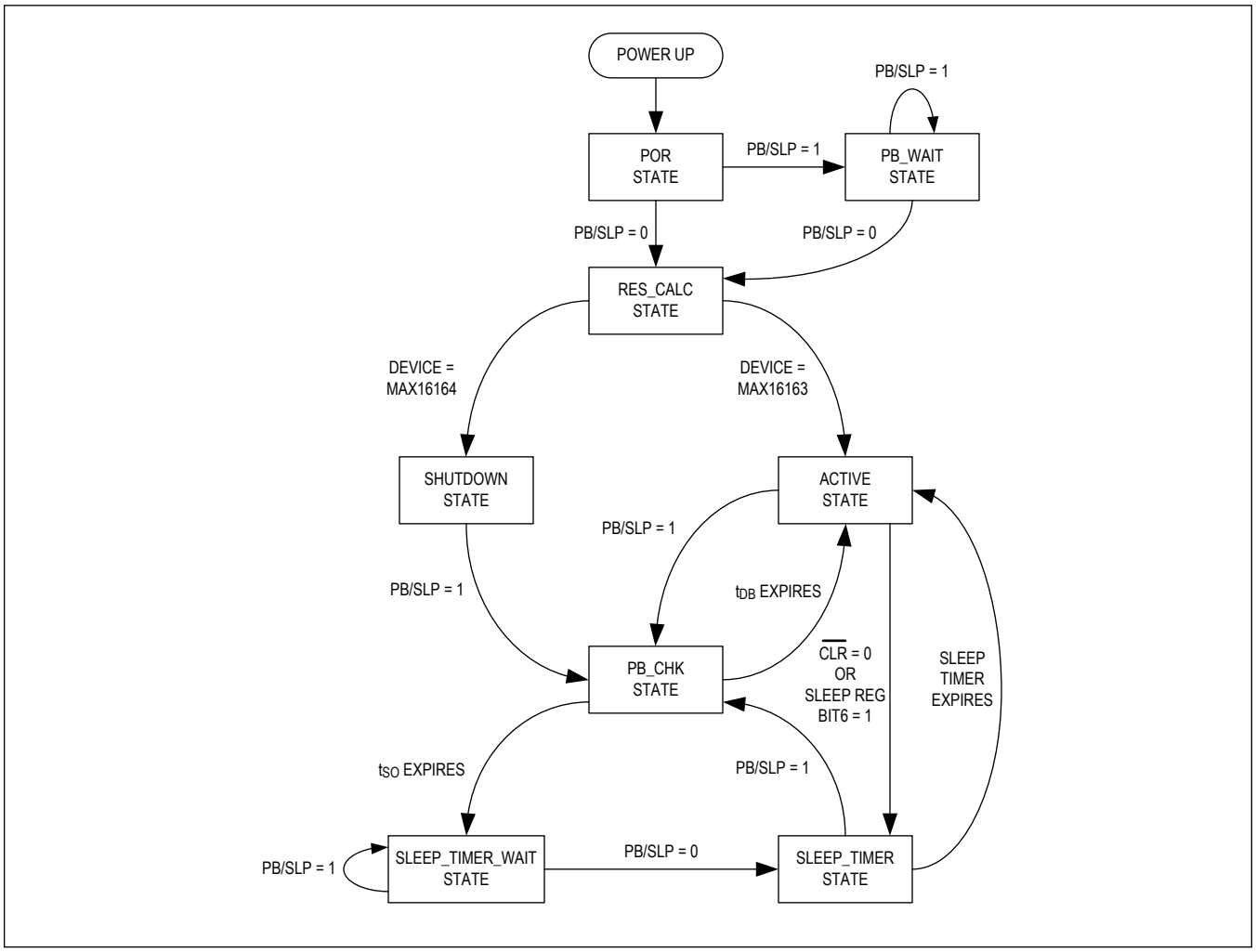



*Figure 2. MAX16163/MAX16164 State Machine Diagram*

### Power On Reset State

After the device has powered up, it enters into the Power On Reset (POR) state and initializes the internal registers. When POR is complete, if the PB/SLP pin voltage is high (i.e., connected to $V_{CC}$ by a pushbutton), the device enters the PB_WAIT state. If the PB/SLP pin voltage is close to 0, the device enters into the RES_CALC state.

In this state, OUT and $\overline{INT}$ are deasserted. $\overline{CLR}$ and PB/SLP are ignored.

### PB_WAIT State

After the POR state is complete, the MAX16163/MAX16164 PB/SLP pin should not be driven by any external signal within 120ms so that the device can measure the resistance between the PB/SLP pin and ground. If the voltage on the PB/SLP pin is high by pressing a pushbutton connected to $V_{CC}$, the device waits in this state until the pushbutton is released.

In this state, OUT and $\overline{INT}$ outputs are deasserted. $\overline{CLR}$ input is ignored.

### RES_CALC State

In this state, the device measures the resistance between the PB/SLP pin and ground. If the resistance is larger than 5.5MΩ, the device is configured as $I^2C$ programmable. If the resistance is less than 5.5MΩ, the device is configured as resistor programmable. The sleep time is programmed as shown in Table 1.

After the resistance is measured, the device enters into the ACTIVE state if the device is the MAX16163. The device enters into the SHUTDOWN state if the device is the MAX16164.

In this state, OUT and $\overline{INT}$ outputs are deasserted. $\overline{CLR}$ input is ignored.

### SHUTDOWN State

This state is specific to the MAX16164. In this state, all the internal circuits except the pushbutton detection circuit stop working in order to minimize power consumption. The user is expected to press the pushbutton to activate the MAX16164. This is useful for the battery seal function for battery operated equipment.

In this state, OUT and $\overline{INT}$ outputs are deasserted, $\overline{CLR}$ input is ignored, and PB/SLP input is low until a button press. After a button press, the device enters into the PB_CHK state.

### ACTIVE State

In this state, OUT is asserted. The device waits for the inputs from the PB/SLP and $\overline{CLR}$ inputs. If a pushbutton press happens, the device enters into the PB_CHK state. If a $\overline{CLR}$ falling edge or an $I^2C$ SHUTDOWN command is received, the device enters into the SLEEP_TIMER state. If a pushbutton press and $\overline{CLR}$ falling edge or an $I^2C$ SHUTDOWN command happen at the same time, the $\overline{CLR}$ falling edge or the $I^2C$ SHUTDOWN command takes precedence over a button press.

### PB_CHK State

After the device is powered up and completes its resistance measurement, any pushbutton press brings the device to this state. In this state, the device checks if the pushbutton press is an invalid press, a short press, or a long press.

If the pushbutton is released (PB/SLP = 0) before the pushbutton debounce time $t_{DB}$ has been passed, the press is invalid (i.e., the press is treated like a noise spike on PB/SLP pin). The device stays in its original state.

If the pushbutton is pressed and the pushbutton debounce time $t_{DB}$ has been passed, the device asserts OUT. If the device enters the PB_CHK state from ACTIVE state, OUT is already asserted and is kept asserted. The device also asserts $\overline{INT}$ output for interrupt pulse duration $t_{INT}$.

If the pushbutton is pressed and the pushbutton shutdown period $t_{SO}$ has been passed, the device deasserts OUT and asserts $\overline{INT}$ for four times the interrupt period, i.e., 4 x $t_{INT}$.

### SLEEP_TIMER State

When entering the SLEEP_TIMER state, the device starts the sleep timer. If the sleep time is set to INFINITE, the sleep timer does not start and the device's internal circuits, except for the pushbutton detection circuit, stop working to minimize the power consumption. The SLEEP_TIMER state with INFINITE sleep time is equivalent to the SHUTDOWN state specific in the MAX16164.

Upon sleep timer expiration, the device asserts OUT and enters into the ACTIVE state.

If the sleep timer expiration and a pushbutton press happen at the same time, the button press takes precedence over the sleep timer expiration; the sleep timer resets, and the state machine enters into PB_CHK state.

### SLEEP_TIMER_WAIT State

The device enters into the SLEEP_TIMER_WAIT state when the device detects the button has been pressed for more than shutdown period $t_{SO}$, but the button has not been released yet. The device waits for the button release to enter into the SLEEP_TIMER state and starts the sleep timer.

## Pushbutton Input Timing

A valid pushbutton press must keep the PB/SLP pin high for equal or more than $t_{DB}$ time. Any press less than $t_{DB}$ is treated as noise. In this document, a button press equal or more than $t_{DB}$ but less than $t_{SO}$ is called a short press, a button press equal or more than $t_{SO}$ is called a long press.

After power up, the MAX16164 is in the SHUTDOWN state to minimize the power consumption. In this state, OUT is deasserted and all circuits except the pushbutton detection circuit stop working. A logic high on the PB/SLP pin wakes up an internal clock, which is used to check if the press is an invalid press, a short press, or a long press. If the press is confirmed to be an invalid press, the internal clock will stop and the device go back to the SHUTDOWN state.

The pushbutton debouncing and press detection diagrams in the SHUTDOWN state (specific in the MAX16164) or the SLEEP_TIMER state with INFINITE sleep time are shown in Figure 3 and Figure 4.

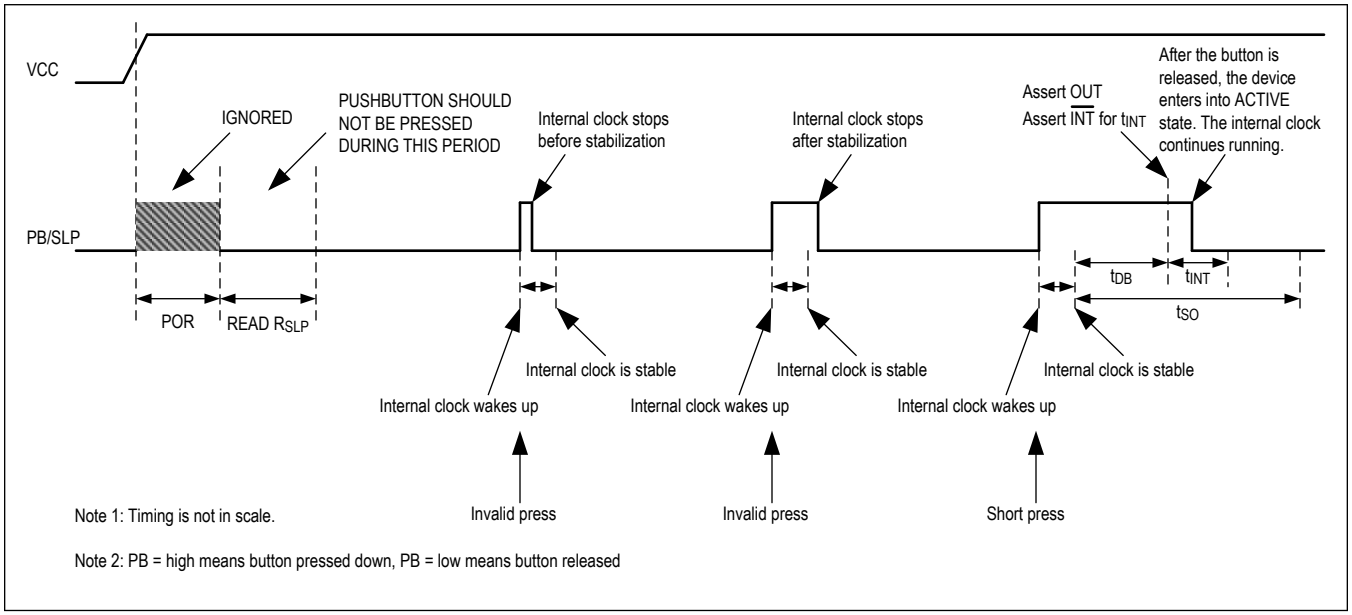



*Figure 3. Invalid and Short Press Detection in SHUTDOWN State and SLEEP_TIMER State with infinite sleep time*

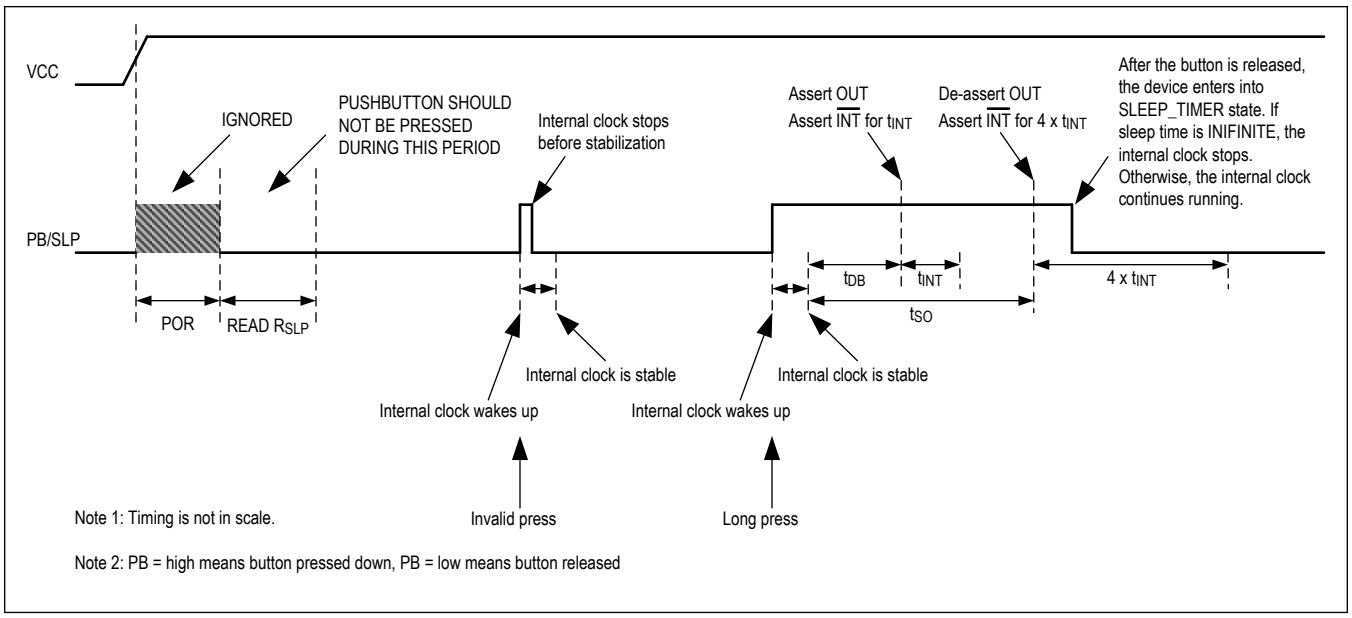



*Figure 4. Invalid and Long Press Detection in SHUTDOWN State and SLEEP_TIMER State with infinite sleep time*

When the devices are in the ACTIVE state or the SLEEP_TIMER state with sleep time not equal to INFINITE, the debouncing and detection is simpler because the internal clock is already running and there is no waking up and stopping of the internal clock.

## $\overline{\text{INT}}$ Output

When the MAX16163/MAX16164 are configured as resistor programmable, an open-drain, active-low $\overline{\text{INT}}$ output is a mirrored event of the pushbutton press. The output can be used as a second function of the pushbutton, sending an interrupt signal to a microcontroller.

A short press generates an active-low pulse for $t_{INT}$ time on the $\overline{\text{INT}}$ pin after the end of $t_{DB}$. A long press generates an active-low pulse for $t_{INT}$ time after the end of $t_{DB}$ first, and then generates another active-low pulse for 4 x $t_{INT}$ time after the end of $t_{SO}$.

The MAX16163/MAX16164 $\overline{\text{INT}}$ output is independent of OUT and has no relationship with OUT.

When the MAX16163/MAX16164 are configured as $I^2C$ programmable, there is no $\overline{\text{INT}}$ output pin or $\overline{\text{CLR}}$ input pin.

$\overline{\text{INT}}$ output timing diagram is shown in Figure 5.

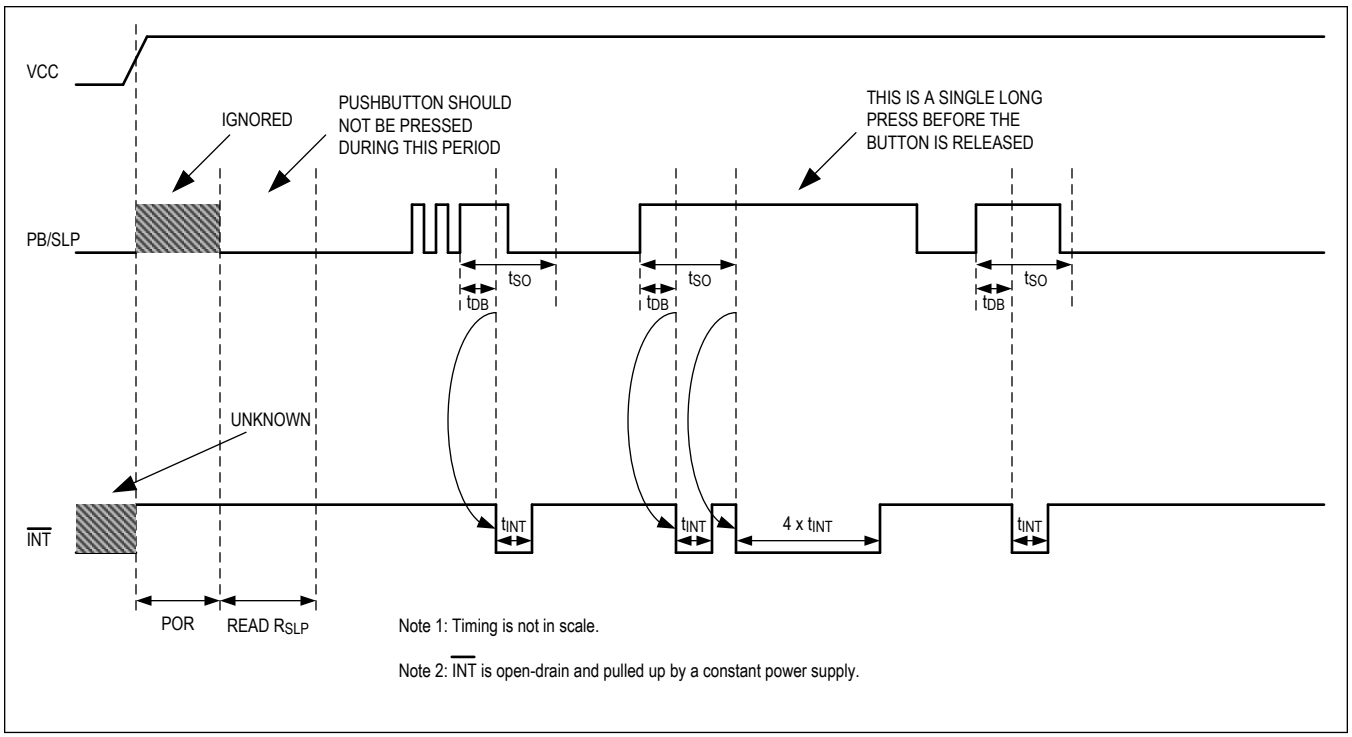



*Figure 5. INT Output Timing Diagram*

## OUT Output

### MAX16163 OUT Output Timing Diagram Without a Pushbutton

Figure 6 shows the OUT output timing diagram of the MAX16163. In the diagram, $\overline{CLR}$ is a hardware signal (in resistor programmable configuration) or an I²C SHUTDOWN command (in I²C programmable configuration).

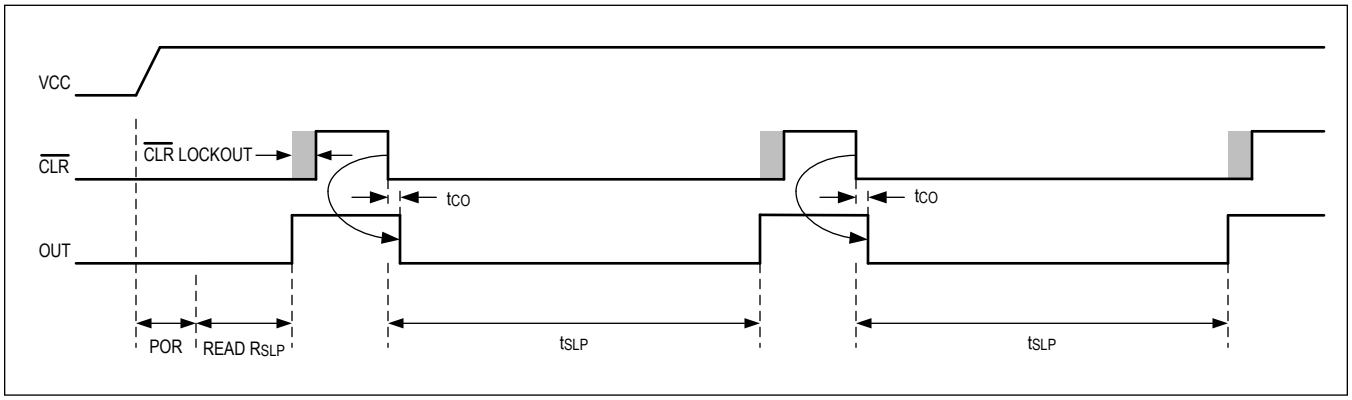



*Figure 6. MAX16163 OUT Output Timing Diagram Without a Pushbutton*

### MAX16163 OUT Output Timing Diagram With Pushbutton

Figure 7 shows OUT output timing diagram of the MAX16163 with a pushbutton connected. In the diagram, $\overline{CLR}$ is a hardware signal (in resistor programmable configuration) or an I²C SHUTDOWN command (in I²C programmable configuration).

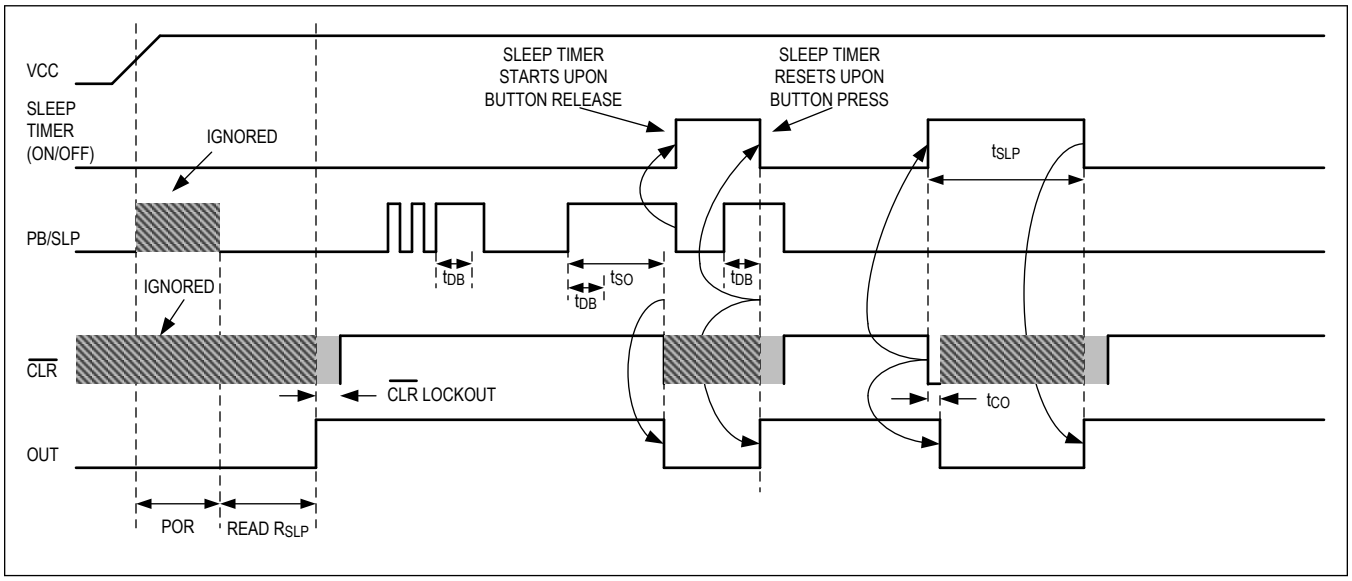



*Figure 7. MAX16163 OUT Output Timing Diagram With a Pushbutton*

### MAX16164 OUT Output Timing Diagram With Pushbutton

Figure 8 shows the OUT output timing diagram of the MAX16164 with a pushbutton connected. In the diagram, $\overline{CLR}$ is a hardware signal (in resistor programmable configuration) or an I²C SHUTDOWN command (in I²C programmable configuration).

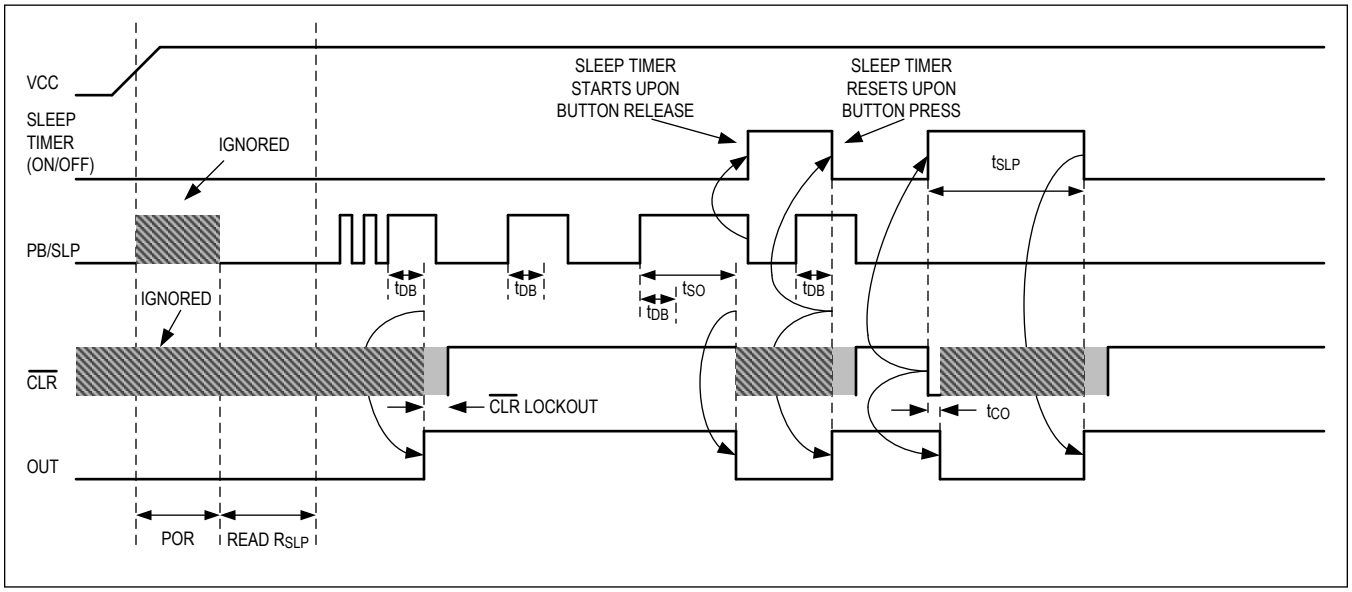



*Figure 8. MAX16164 OUT Output Timing Diagram With a Pushbutton*

### A Special Case When OUT is Deasserted and A Long Press Happens

When OUT is deasserted (the SHUTDOWN state or the SLEEP_TIMER state), if a short press happens, the MAX16163/MAX16164 assert OUT first. If the button is continuously pressed and $t_{SO}$ has passed, the MAX16163/MAX16164 deassert OUT again. After that, even if the button is still pressed, there won't be any OUT state changes. The device enters into the SLEEP_TIMER_WAIT state for the button to release, then starts the sleep timer.

## I²C Serial Data Bus

### I²C Bus Operations

The MAX16163/MAX16164 are compatible with a bidirectional I²C bus and data transmission protocol. A device that sends data onto the bus is defined as a transmitter and a device receiving data is defined as a receiver. The device that controls the message is called a master. The device that is controlled by the master is a slave. The bus must be controlled by a master device that generates the serial clock (SCL), controls the bus access, and generates the START and STOP conditions. The MAX16163/MAX16164 operate as slaves on the I²C bus. Connections to the bus are made through the open-drain I/O lines SDA and SCL. The MAX16163/MAX16164 work in standard mode (100kHz maximum clock rate).

### Detailed I²C Timing Diagram

The detailed timing diagram of various electrical characteristics is shown in Figure 9.

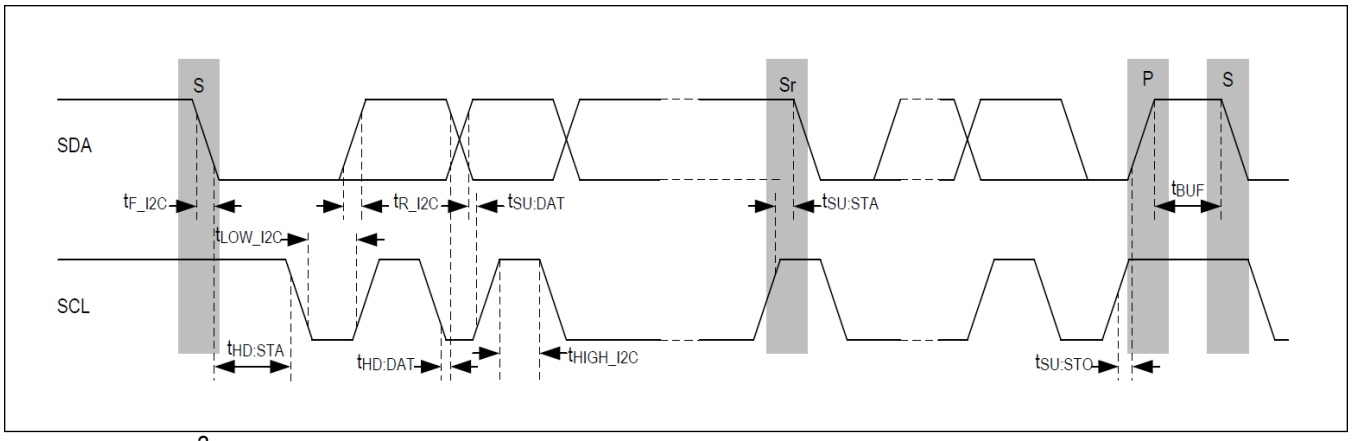



*Figure 9. Detailed I²C Timing Diagram*

### I²C Slave Address

The 7-bit slave address is 0x23.

### Device Register and Operation

The Sleep Time register (register address 0x00) is the only device register that a microcontroller can read from and write to. The register content and operations are shown in Figure 10.

| BIT 7 | BIT 6 | BIT 5 | BIT 4 | BIT 3 | BIT 2 | BIT 1 | BIT 0 |
|---|---|---|---|---|---|---|---|
| BUS STATUS | OUT | SLEEP TIME INDEX (SEE TABLE 1 FOR SLEEP TIME VALUES) | | | | | |

BIT 7: read only, I2C bus status.
If BIT 7 = 0, I2C write operation is allowed. If BIT 7 = 1, I2C write operation is not allowed.

BIT6: clear-after-write register.
If BIT 6 = 0, OUT does not change. If BIT 6 = 1, de-assert OUT after write operation.

*Figure 10. Device Register and Operation*

In I²C configuration, the hardware $\overline{CLR}$ pin is not available. The microcontroller writes the register with bit 6 = 1 to deassert OUT. Any register write overrides the sleep time with the new register value. It's recommended to read the register first and then mask bit 6 and write with the new register value to keep the sleep time unchanged.

There are two standard I²C operations: register write and register read. The I²C register is accessible anytime, no matter if OUT is asserted or deasserted.

### Register Write Operation

To write the sleep time register, the master sends a start condition on the bus with the MAX16163/MAX16164 address as well as the last bit (the R/$\overline{W}$ bit) set to 0, which signifies a write. After the MAX16163/MAX16164 sends the acknowledge bit, the master then sends the register address (0x00). The MAX16163/MAX16164 acknowledges again, letting the master know it is ready. After this, the master starts sending the register data to the MAX16163/MAX16164. The master terminates the transmission with a STOP condition. Figure 11 shows the format of a single write register operation.

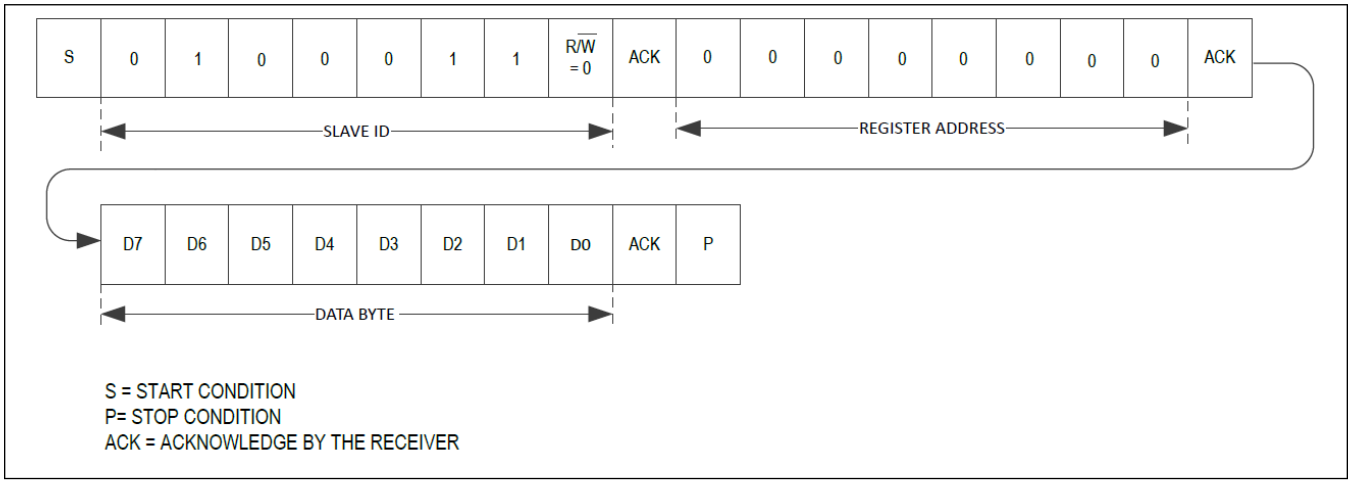



*Figure 11. Register Write Operation*

### Register Read Operation

The master sends the slave address (0x23) with the R/$\overline{W}$ bit equal to 0 (signifying a write), followed by the register address (0x00). Once the MAX16163/MAX16164 acknowledges this register address, the master sends a START condition again, followed by the slave address with the R/$\overline{W}$ bit set to 1 (signifying a read). This time, the MAX16163/MAX16164 acknowledges the read request, and the master releases the SDA bus and continues supplying the clock to the MAX16163/MAX16164. In this transaction, the master becomes the master-receiver, and the MAX16163/MAX16164 becomes the slave-transmitter. Once the master has received the byte, it sends a NACK, signaling to the slave to halt communications and release the bus. The master then sends a STOP condition.

Figure 12 shows the format of a single register read operation.

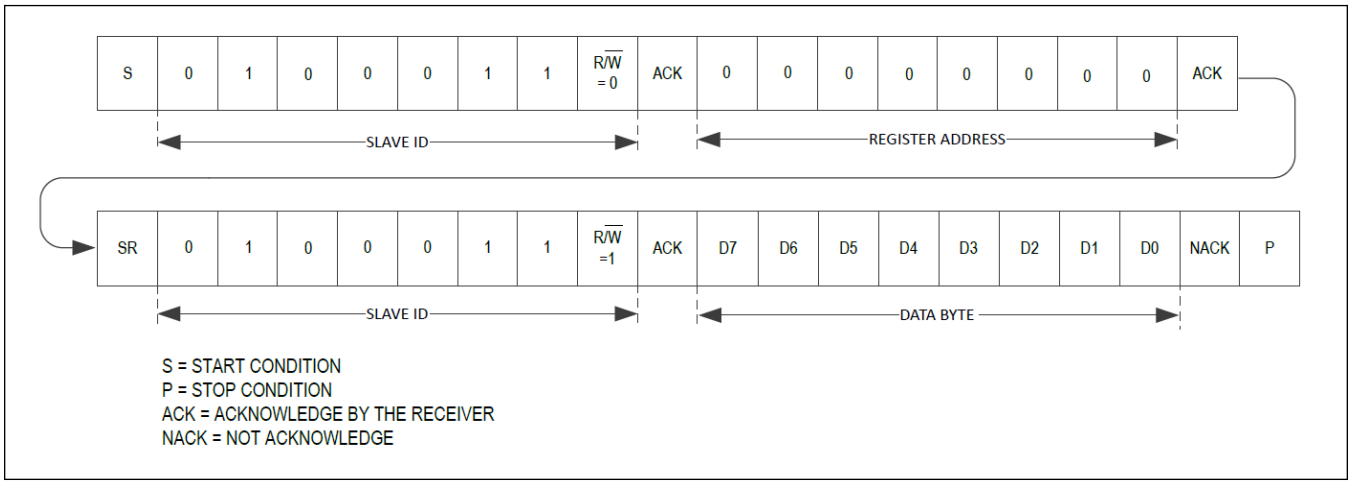



*Figure 12. Register Read Operation*

### Selector Guide

MAX1616_

| SUF | POWER-UP STATE |
|---|---|
| 3 | ACTIVE |
| 4 | SHUTDOWN |

| SUF | TEMPERATURE RANGE |
|---|---|
| A | -40°C TO +125°C |

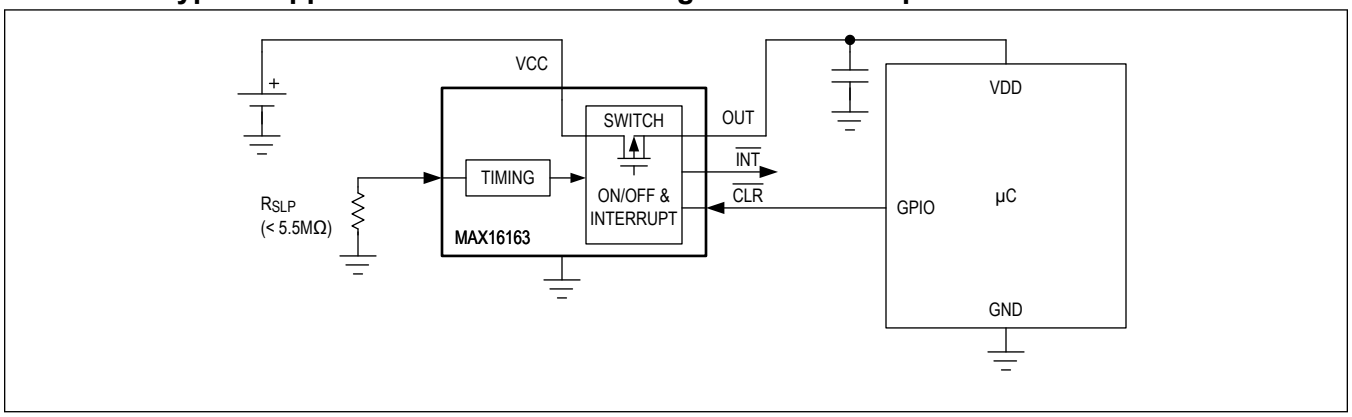
| SUF | PACKAGE |
|---|---|
| NT | 6 WLP |
| LT | 6 µDFN |

| SUF | DEFAULT SLEEP TIME WHEN CONFIGURED AS I2C PROGRAMMABLE |
|---|---|
| 00 | 100ms |
| 01 | 200ms |
| 02 | 400ms |
| 03 | 600ms |
| 04 | 800ms |
| 05 | 1s |
| 06 | 2s |
| 07 | 4s |
| 08 | 6s |
| 09 | 8s |
| 0A | 10s |
| 0B | 20s |
| 0C | 40s |
| 0D | 1min |
| 0E | 2min |
| 0F | 4min |
| 10 | 6min |
| 11 | 8min |
| 12 | 10min |
| 13 | 20min |
| 14 | 40min |
| 15 | 1h |
| 16 | 2h |
| 17 | 4h |
| 18 | 6h |
| 19 | 8h |
| 1A | 10h |
| 1B | 12h |
| 1C | 16h |
| 1D | 20h |
| 1E | 24h |
| 1F | INFINITE |

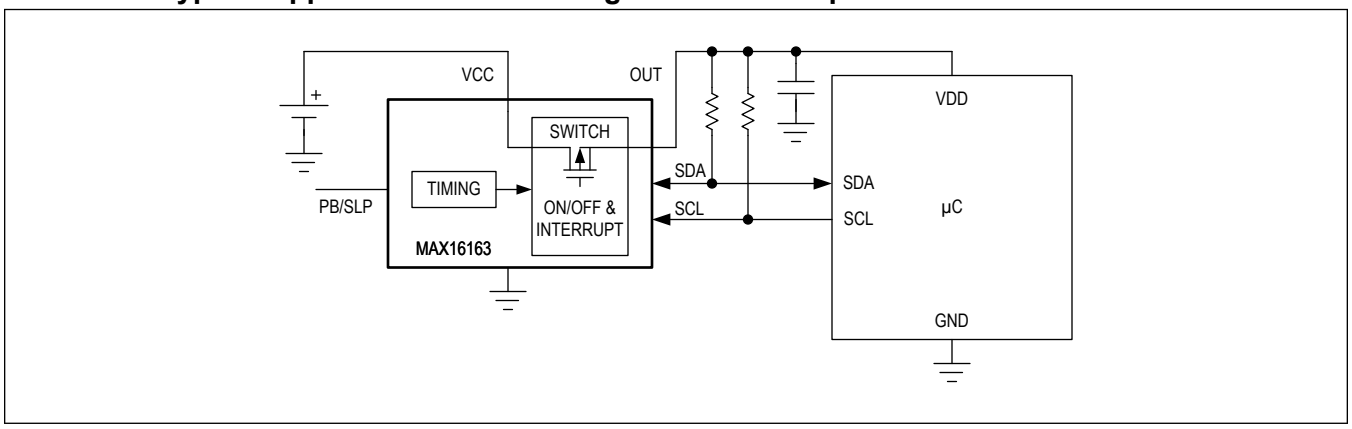
*Figure 13. MAX16163/MAX16164 Selector Guide*

## Typical Application Circuits

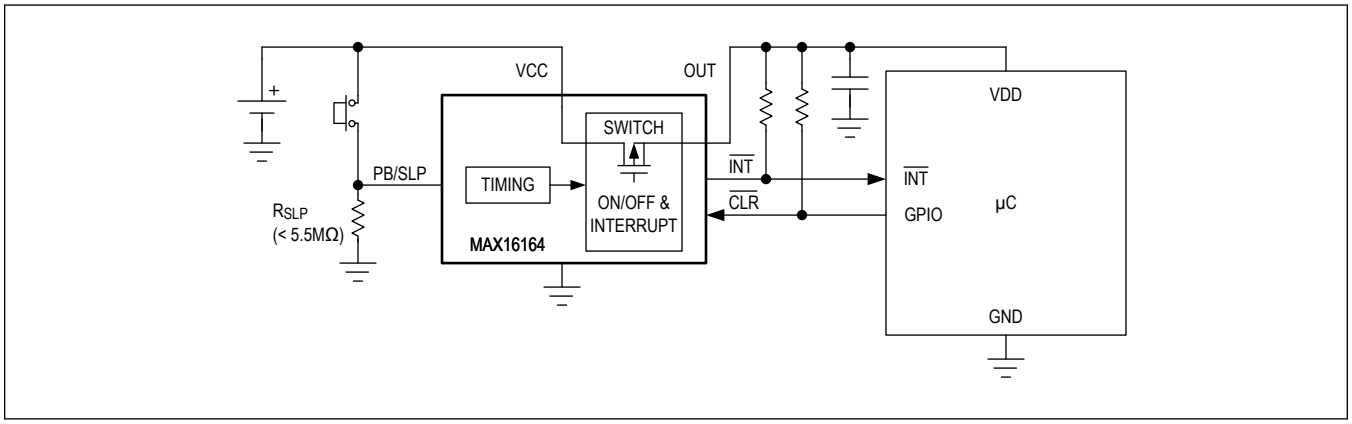
### MAX16163 Typical Application with Resistor Programmable Sleep Time and no Pushbutton




### MAX16163 Typical Application with I²C Programmable Sleep Time and no Pushbutton

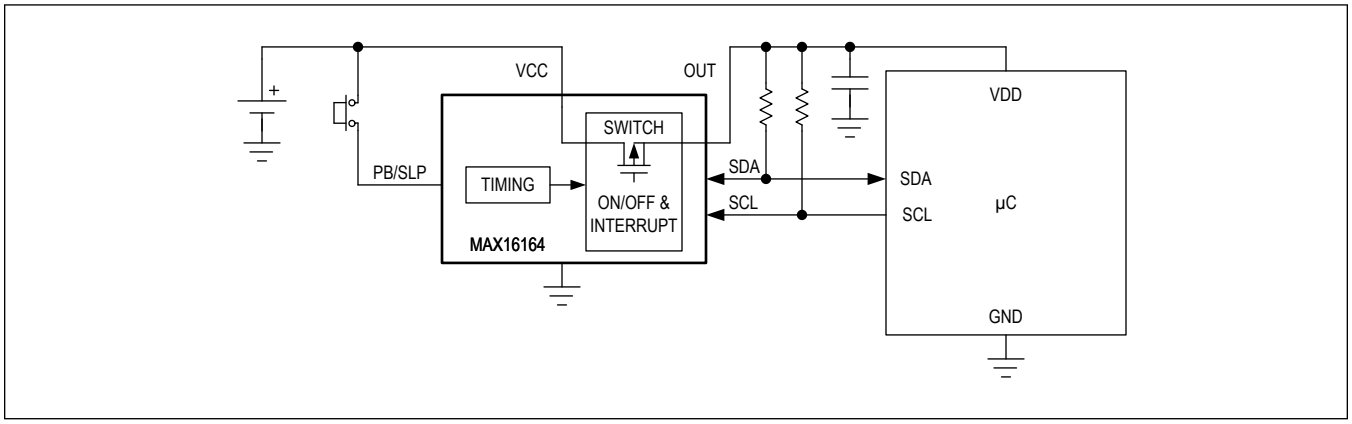



### MAX16164 Typical Application with Resistor Programmable Sleep Time and Pushbutton



## Typical Application Circuits (continued)

### MAX16164 Typical Application with I²C Programmable Sleep Time and Pushbutton




## Ordering Information

| PART NUMBER | POWER-UP STATE | DEFAULT SLEEP TIME WHEN CONFIGURED AS I²C PROGRAMMABLE | TEMP RANGE | PIN-PACKAGE |
|---|---|---|---|---|
| MAX16164ANT0D+T | Shutdown | 1 minute | -40°C to +125°C | 6 WLP |
| MAX16163ANT0D+T | Active | 1 minute | -40°C to +125°C | 6 WLP |
| MAX16164A----+T * | Shutdown | See Figure 13 | -40°C to +125°C | 6 uDFN |
| MAX16163A----+T * | Active | See Figure 13 | -40°C to +125°C | 6 uDFN |

*+Denotes a lead(Pb)-free/RoHS-compliant package.*

*T = Tape and reel.*

**Future product—contact factory for availability.*

## Revision History

| REVISION NUMBER | REVISION DATE | DESCRIPTION | PAGES CHANGED |
|---|---|---|---|
| 0 | 9/21 | Release for Market Intro | — |
| 1 | 10/21 | Updated *Ordering Information* table | 24 |

# Mouser Electronics

Authorized Distributor

Click to View Pricing, Inventory, Delivery & Lifecycle Information:

Analog Devices Inc.:

MAX16164ANT0D+ MAX16163ANT0D+ MAX16164ANT0D+T MAX16163ANT0D+T